

# Time-over-threshold (TOT) studies with the DPTS

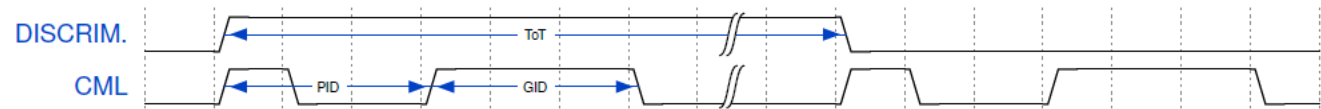
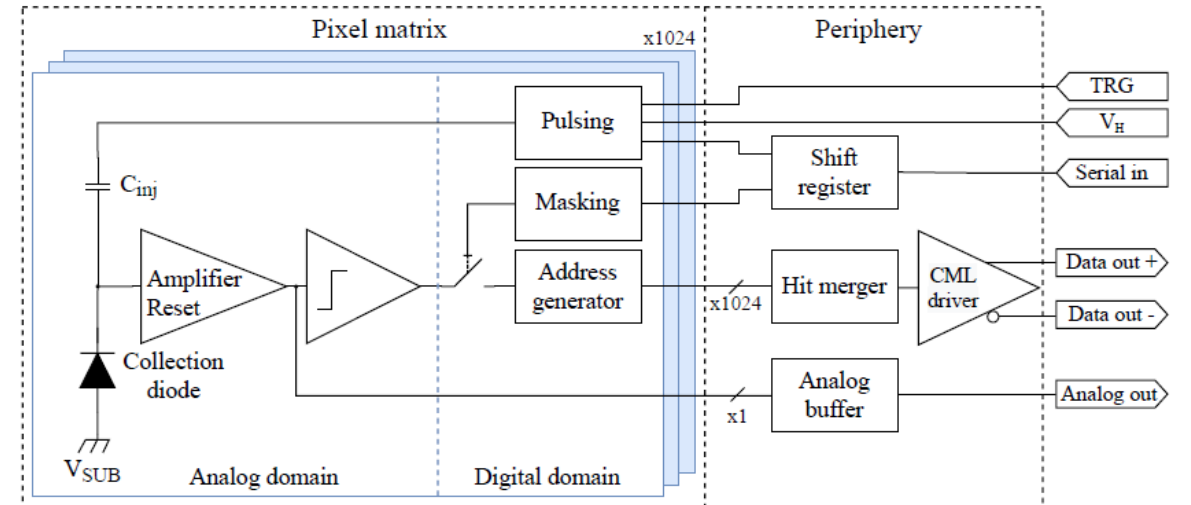
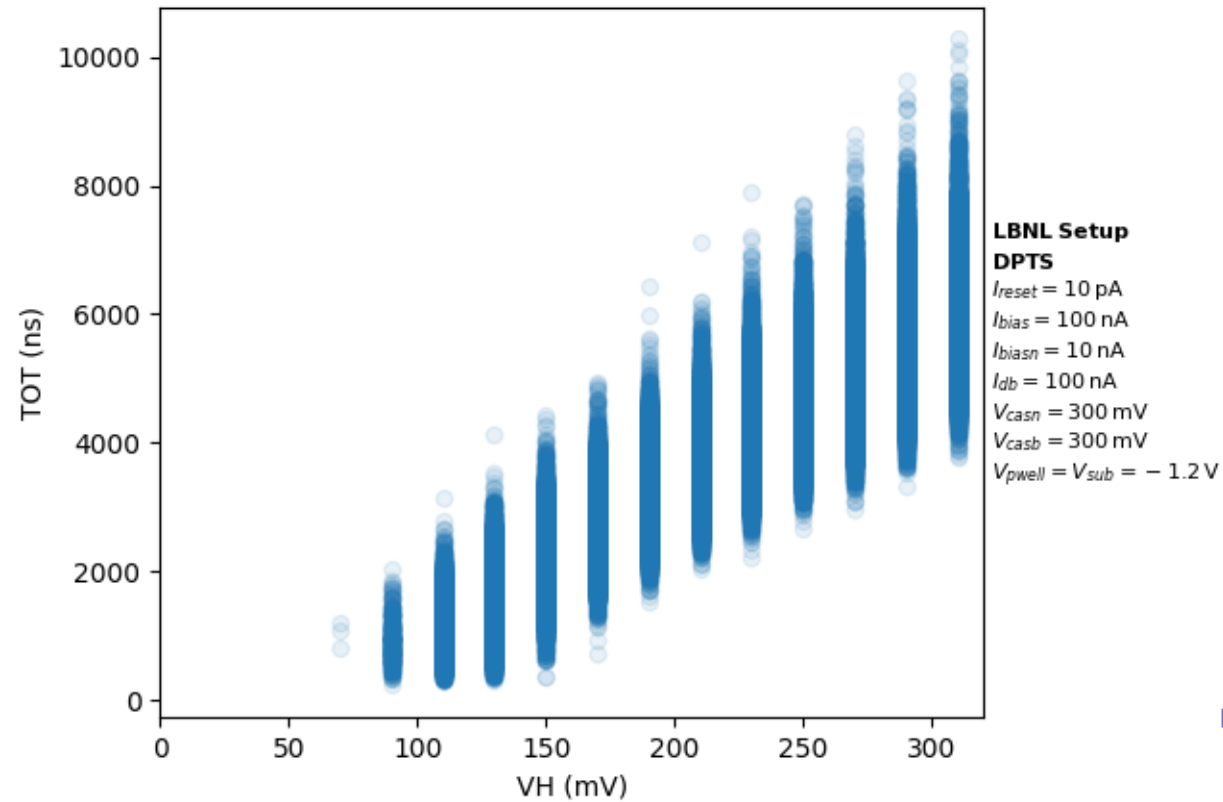
Barak Schmookler

# Task list for DPTS studies

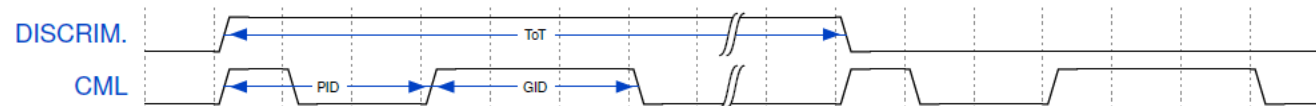
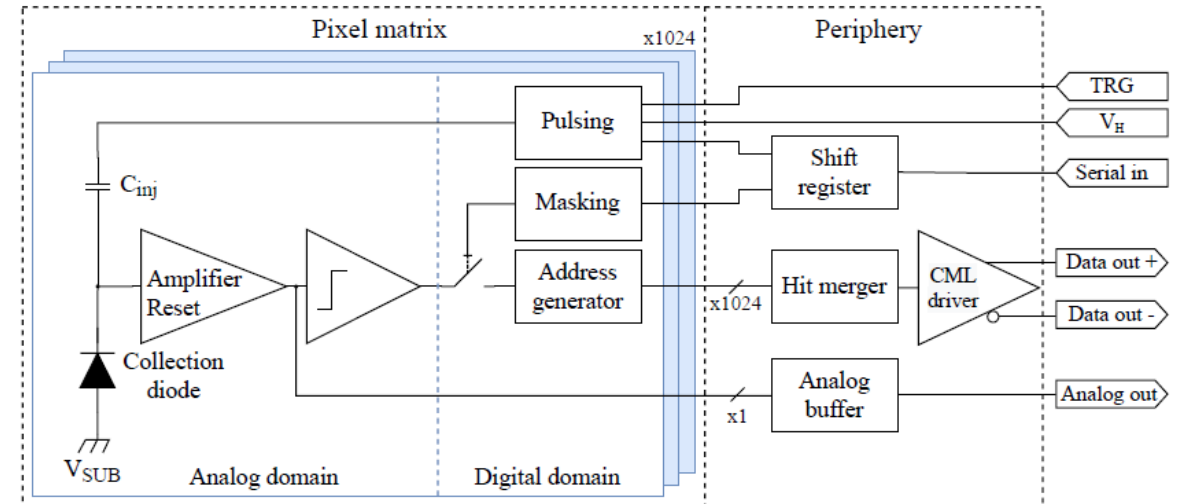
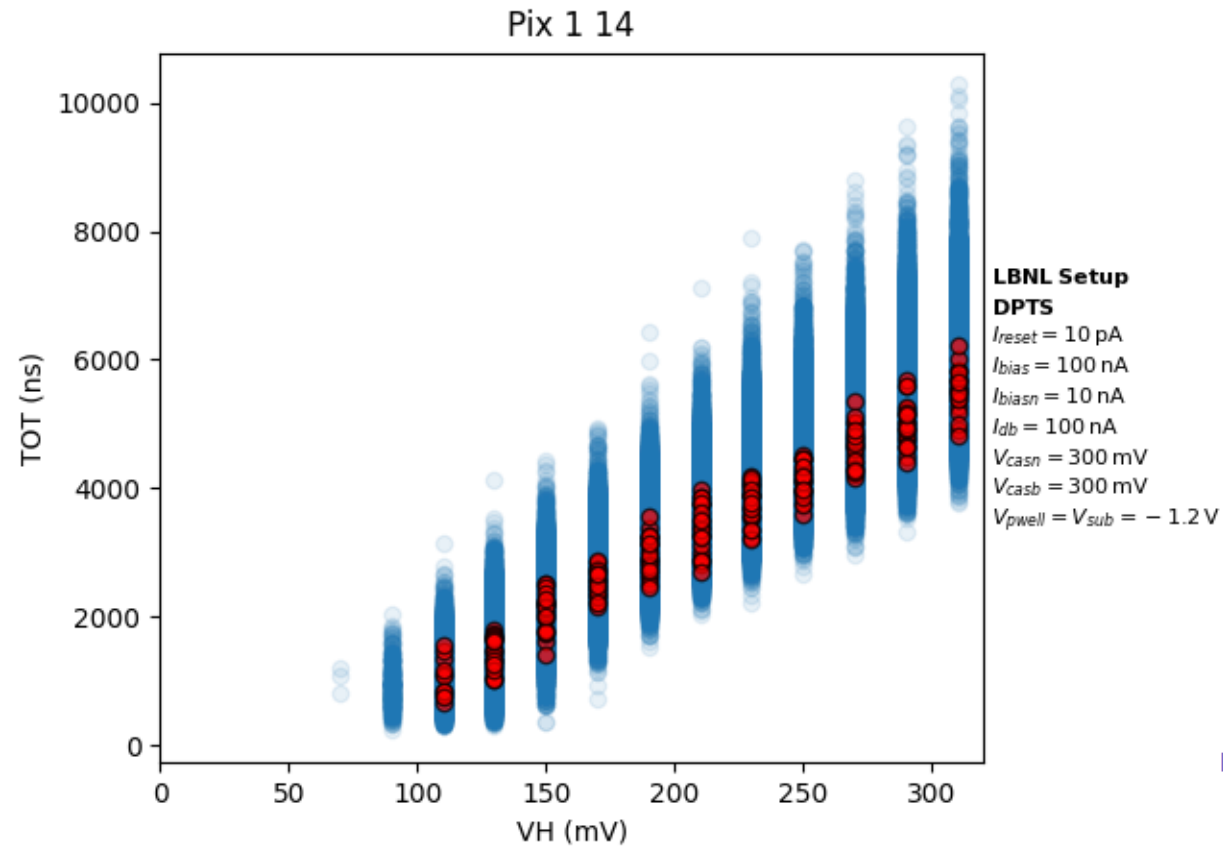
## Laboratory measurements

Task	Assigned	Timeframe	Details
Power consumption study	Trieste/CERN	24th April	Investigate the performance of the chip as a function of IBIAS. Look into the threshold, noise, FHR, <u>ToT</u> , and <u>ToA</u> . Also, investigate optimal working points for low IBIAS values. Only needed for VBB = -1.2 V
2e15, 5e15 and 1e16 chips	CERN	?	Investigate if the chips work: do at lower temp (< 15°C) and higher IRESET (> 70 pA), commission controlled environment setup
Bent DPTS	Trieste	?	With WP4 investigate bent DPTS chips
Pixel-to-pixel variation in threshold and leakage current	Trieste	?	See variations in chip biases pixel-to-pixel when all pixels are tuned to the same threshold
Study <u>ToT</u> pixel-to-pixel variation	?	?	What is the reason for such a large <u>ToT</u> RMS and pixel-to-pixel variation? Correlate the difference with other parameters
Remeasure all plots in paper with different chips	?	?	Remeasure all threshold, FHR and <u>ToT</u> dependence as well as Fe55 spectra shown in the paper for different chips
Pulsing capacitance measurement	?	?	Look at chip-to-chip and pixel-to-pixel variations
FHR and thermal noise study	?	?	Investigate sources of FHR: thermal, telegraph. Hot pixels. Chip-to-chip study
Dead pixels	?	?	Study pixels unresponsive to pulsing and external stimuli.
Power consumption	?	?	Study the chip performance at different power consumption levels
Characterise the CML	ORNL	?	Performance as a function of BBIAS current
Regularly measure TID chips	CERN	Ongoing	Look into annealing effects on the chips: threshold, noise, noise occ, PID/GID clusters
Test different splits	?	?	Study the behaviour of different splits
Injecting noise via vbb or pwell	?	?	Study the chip behaviour with different noise levels
Separating PWELL and SUB	?	?	Study the chip behaviour with separate PWELL and SUB
Look at chip-to-chip variations	?	?	Study the chip-to-chip behaviour of currents, thresholds, noise and leakage current
DPTS timing back-to-back	CERN	?	Use Sr90 to investigate the timing of two DPTS chips back-to-back (on hold for now, needs supplement with a testbeam measurement)

# TOT vs. Injected Charge – the large observed pixel-to-pixel variation is not understood

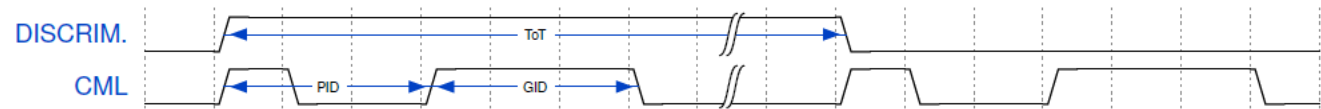
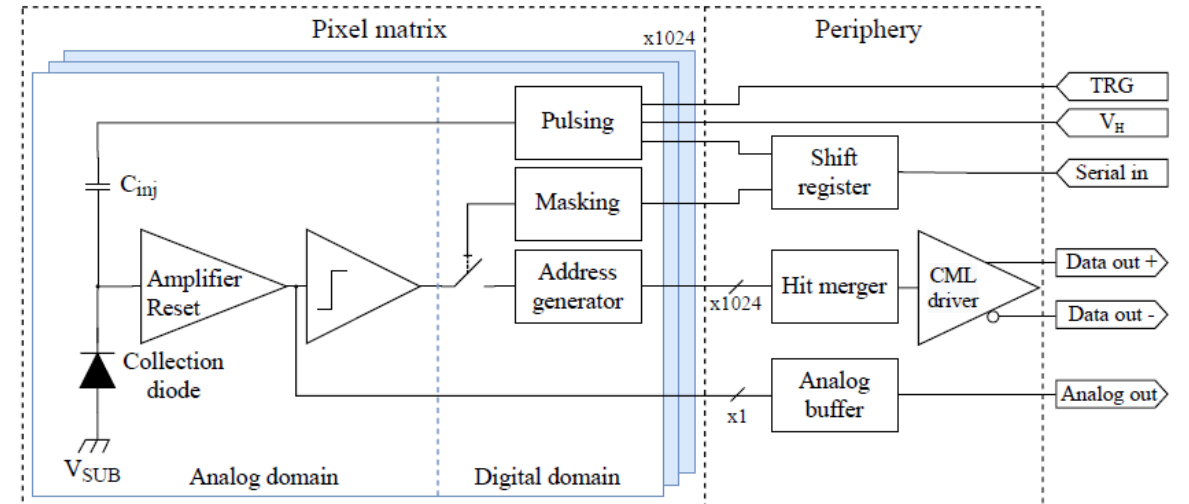
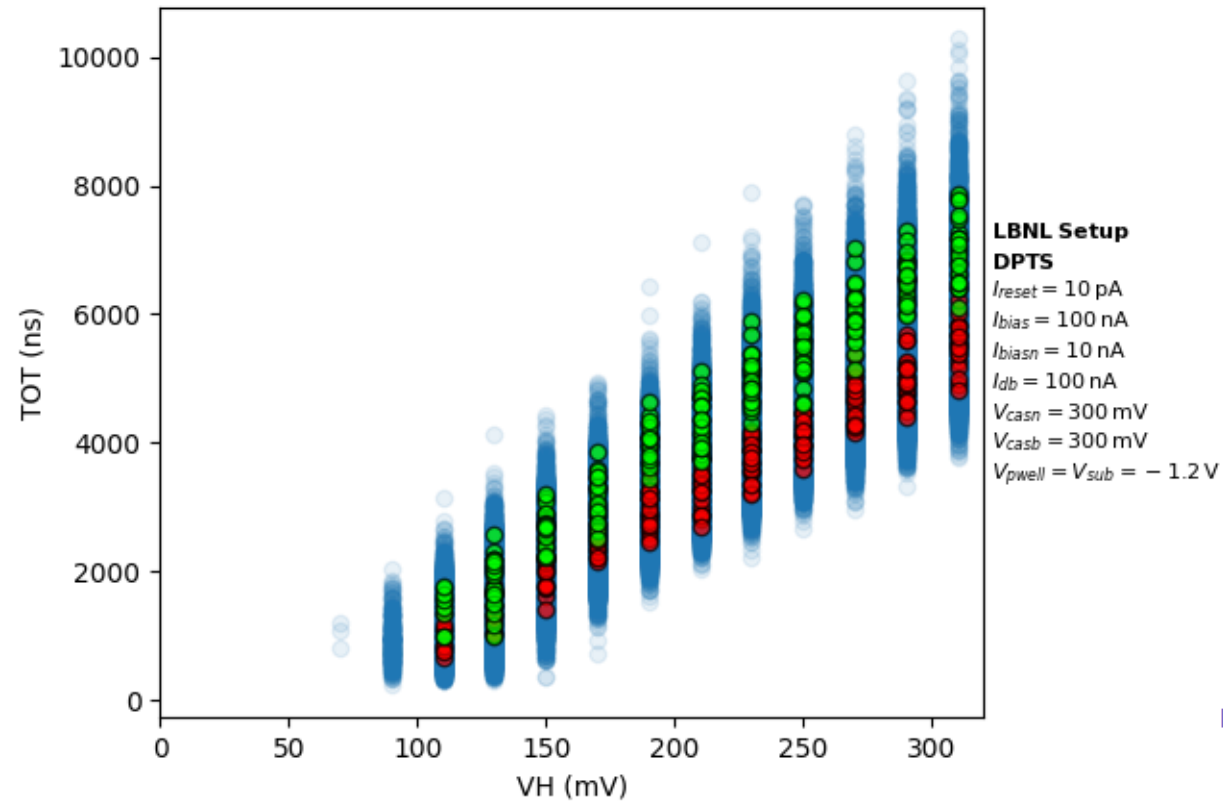


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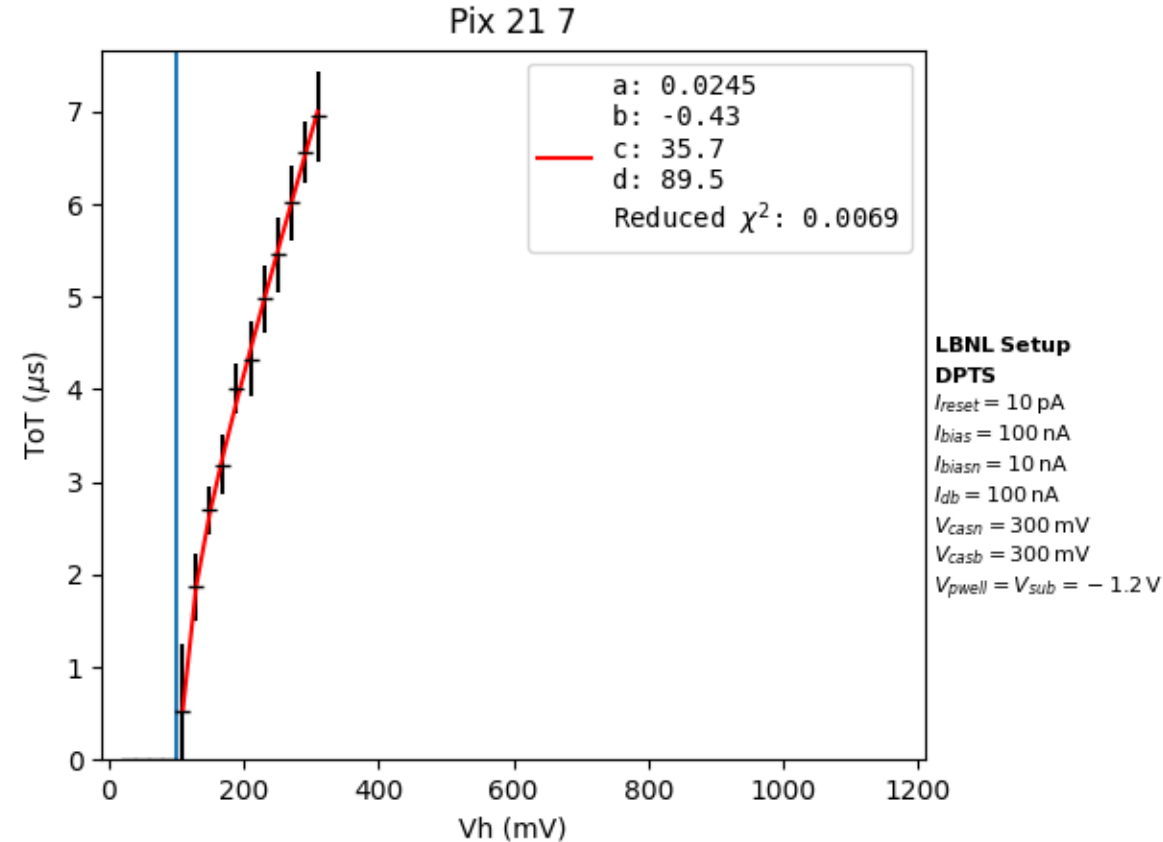
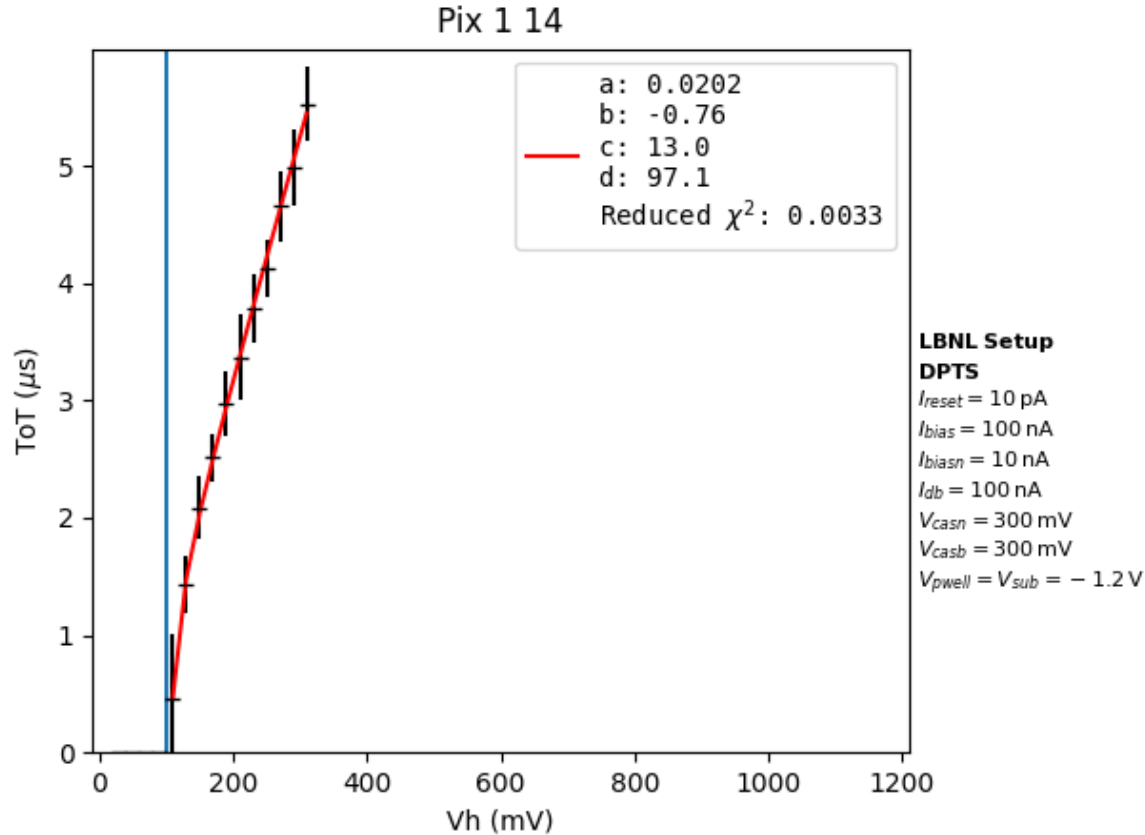


# TOT vs. Injected Charge – the large observed pixel-to-pixel variation is not understood

Pix 1 14 and Pix 21 7



# What is a good way to characterize this variation?

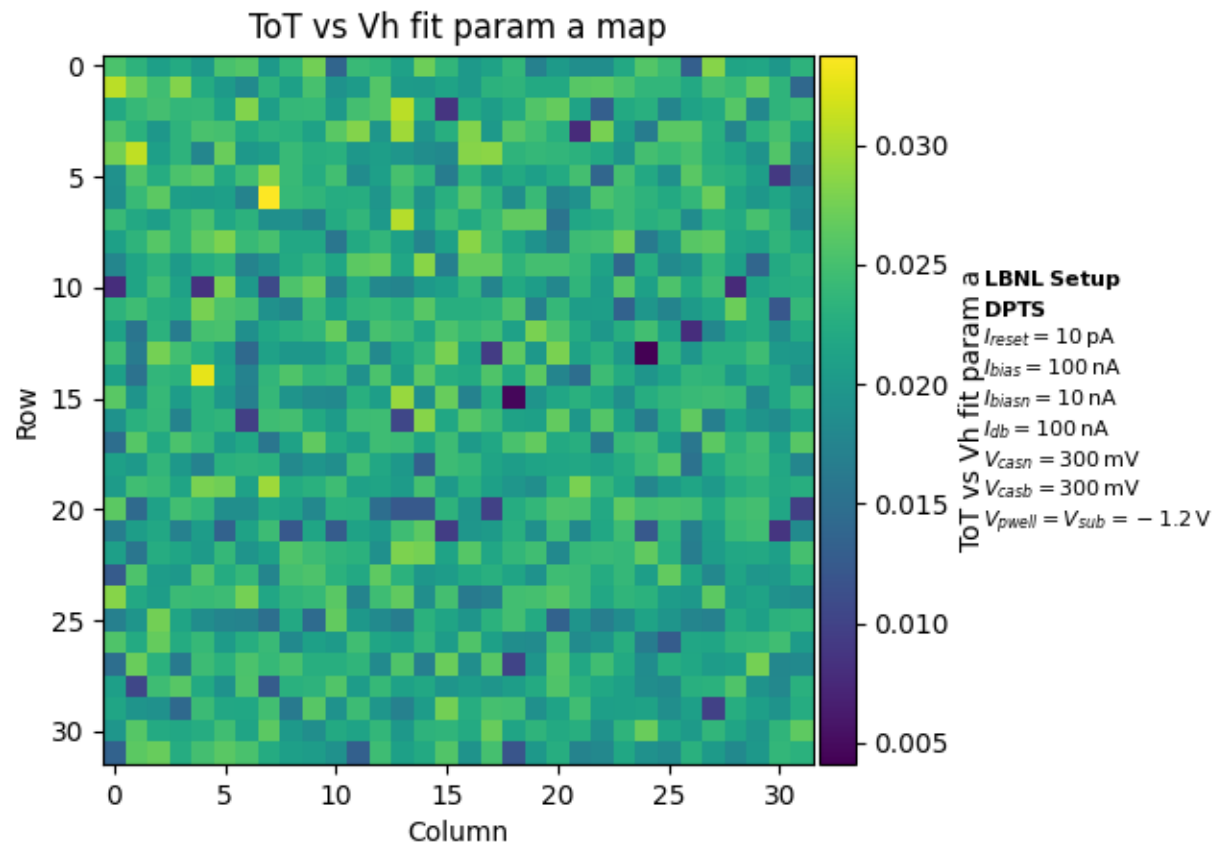
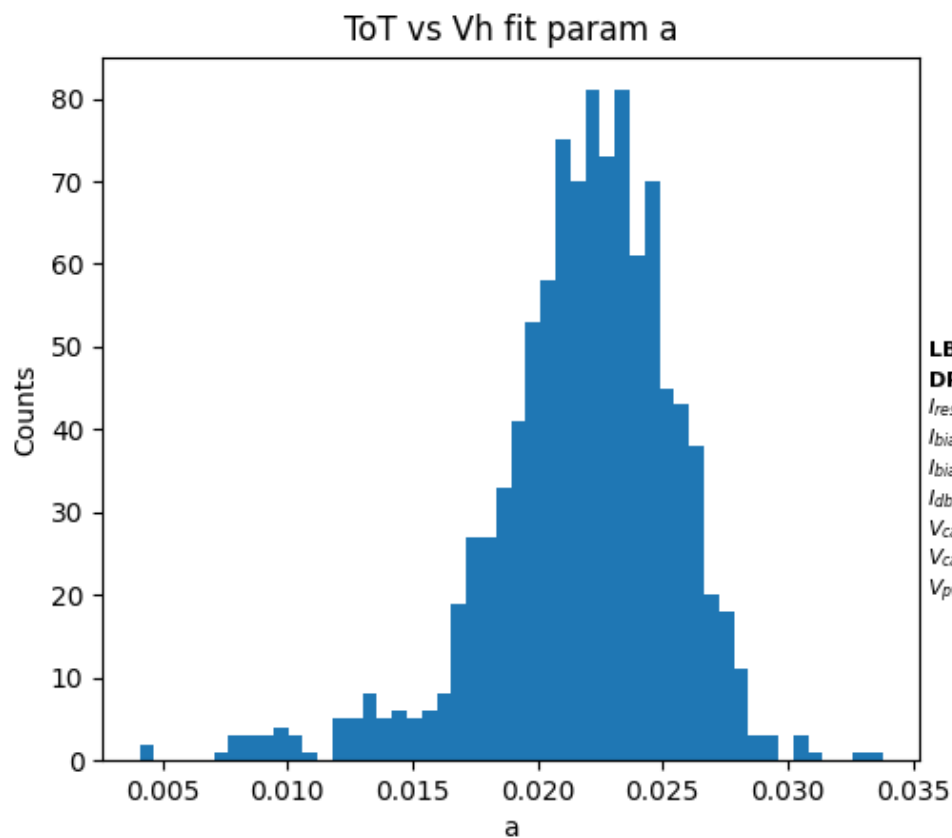


In these plots,  $y$  is the average TOT for the 25 measurements at a given injected charge ( $V_H$ ). The  $y$  error bar shown is the standard deviation of those 25 measurements. It is not the standard error of the mean.

I fit with the function:

$$y = ax + b - \frac{c}{x - d}$$

# Comparison of slope for all pixels



I fit with the function:

$$y = ax + b - \frac{c}{x - d}$$

## Next steps

1. Think about what are the best 'figure of merits' to use to characterize the pixel-to-pixel variation.
2. Take data with a wider range of injected charge. So far, I only go up to  $V_H = 300$  mV.
3. Repeat the TOT vs. injected charge scans for other voltage and current settings. Need to figure out how to automate the process a bit.