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PCIe and VME low latency data transfer in scalable LLRF systems

The design of a digital LLRF system for SwissFEL with repetition rate of 100 Hz and distributed ADC channels demands for a concept with high-speed and low latency data transfer links and a variable number of connected boards. The modular unit of digital part of the LLRF system is a VME board with PCI express based infrastructure between FPGA, CPU and external PCI express devices. Two FMC mezzanine slots are available for connection of ADC/DAC cards. Since feedback algorithms shall run on a central carrier board, where the DAC mezzanine card is located, the data transfer of all required ADC's has to be implemented in a flexible manner with lowest possible latency. Performance figures for latency values for different link types (VME bus, PCI express) as a function of data packet size are presented.

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