

A Flexible High-Speed Architecture for Digital Signal Processing With Applications for Transverse Feedback

A 4GSa/s signal processing system has been developed for proof of concept transverse intra-bunch closed loop feedback control studies at the CERN SPS. This system contains a beam pickup, analog front end receiver, signal processor, back end driver, power amplifiers and kicker structure. The main signal processing function is performed digitally, using very fast (4GSa/s) data converters to bring the system signals into and out of the digital domain. The digital signal processing function itself is implemented in an FPGA allowing for maximum speed and flexibility, utilizing the FPGA's DSP-specific resources to implement FIR based control filters. In addition to the feedback function, an excitation feature was added allowing the system to run as a bursted arbitrary waveform generator. These operating modes are complemented with a set of diagnostics, which includes a programmable snapshot memory for recording of input data. This system has served well in proof of concept studies at the SPS and will be expanded with further capabilities and features. The signal processor utilizes commercial silicon and is a modular design consisting of commercial and custom components. This approach allowed for a rapidly-developed prototype to be delivered in a short time with very limited resources. Though designed for a specific purpose, its topology and FPGA implementation allow it to be used for general-purpose applications beyond that of its original design. This paper describes the design and implementation of this system, with an emphasis of the flexibility of the architecture for other applications.

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