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LLRF Using SoC FPGAs in a Multiple Development Tool Environment

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The shrinking silicon geometries in FPGA technology provides the designer today with greatly increased computing and logic resources in a compact low cost package. Application class floating point hard processor cores with a number of high speed peripherals are tightly integrated with FPGA logic on a single chip. The new FPGA architectures come with several high level design and debugging tools that promise to reduce the development effort and time for complex systems. Multiple tools such as, QuartusII, Qsys, DSP builder, Nios EDS, SoC EDS from Altera, Matlab and Simulink from Mathworks, DS-5 development environment from ARM, Linux or VxWorks operating system kernel builders for the ARM, need to be used to design with these new FPGA chips. In the context of a system design for a LLRF system, these new tools and FPGA's are evaluated for their ease of use and the new system architectures that could be adopted for future systems. A complete LLRF system is designed with an Altera 28-nm CycloneV SoC chip with 110k logic elements and dual 800 MHz ARM processors and the tools and new architecture options are explored.

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